UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,435	01/10/2002	Takashi Kariya	217883US3PCT	6548

22850 7590 09/16/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
GOFF II, JOHN L	
ART UNIT	**PAPER NUMBER**
1733	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,435	KARIYA, TAKASHI	
	Examiner	Art Unit	
	John L. Goff	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/20/04 has been entered. The objections to the specification have been overcome.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102/103

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Gerber et al. (U.S. Patent 5,401,913).

Gerber et al. disclose a method for manufacturing a multilayer circuit board. Gerber et al. teach forming a single circuit board by providing an insulating layer (e.g. 10 of Figure 8), forming a conductor layer on one side of the insulating layer (e.g. 12, 16, and 22 of Figure 8), forming a via hole (e.g. 18 of Figure 5) through the insulating layer to the conductor layer, filling at least part of the via hole with a first conductor material (e.g. 20 of Figure 8) wherein at least part of the upper surface of the conductor material is lower than the upper surface of the insulating substrate, and then forming a conductive bump (e.g. 22 of Figure 8) on the first

conductor material from a second conductive material having a low melting point such that the bump projects from the upper surface of the insulating substrate (Figures 1-8 and Column 3, line 1 and Column 4, lines 1, 9-12, 42-43, and 63-68 and Column 5, lines 1-5 and 15-21). Gerber et al. teach manufacturing an interconnect (part of the final multilayer circuit board) by applying heat and pressure to a multilayer stack comprising a plurality of single circuit board layers (as described above) having a lower outermost copper conductor layer (e.g. 50 of Figure 9 wherein the conductor layer has a uniform thickness throughout) with a layer of adhesive (e.g. 24 of Figure 9) interposed between each layer in the stack such that the layers of the stack are bonded to form an interconnect used in a multilayer circuit board with the conductive bump of each circuit board connected to the conductor layer of an adjacent circuit board (Figures 9 and 10 and Column 5, lines 46-55 and 61-68 and Column 6, lines 1-3 and 12-21 and Column 7, lines 18-28). It is noted Figures 9 and 10 of Gerber et al. do not depict an upper outermost copper conductor layer. However, Gerber et al. teach the interconnect of Figure 9 is connected to rigid substrates such as a circuit board having conductive (e.g. copper) pads to form an integral, operable (i.e. electrically interconnected) multilayer such that the limitation requiring an upper outermost copper conductor layer appears to be met (Figure 11 and Column 5, lines 67-68 and Column 6, lines 1-3 and Column 7, lines 18-23). Additionally, Figure 11 of Gerber et al. show manufacturing an integral, operable (i.e. electrically interconnected) multilayer circuit board (e.g. 70 of Figure 11) comprising a single circuit board layer as described above (e.g. 72, 76, 80, 82, 84, and 86 of Figure 11) bonded to a copper conductor pad layer (e.g. 78 of Figure 11) of a circuit board (e.g. 74 of Figure 11) such that the limitation appears to be met (Figure 11 and Column 6, lines 58-65). Furthermore, it would have been obvious to one of ordinary skill in the

art at the time the invention was made that the interconnect of Figure 9 taught by Gerber et al. is only useful as a multilayer circuit board when connected to an additional outer conductor layer (e.g. formed of copper) of an additional substrate such as a circuit board to form an integral, operable (i.e. electrically interconnected) multilayer circuit board such that it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an upper outermost conductor (e.g. copper) layer and adhesive layer at the time of pressing the multilayer stack as only the expected results would be achieved.

Claim Rejections - 35 USC § 103

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gerber et al. in view of either one of Fukukawa et al. (JP 08293677 and the English abstract), Bohn (U.S. Patent 6,537,412), or Johnston (U.S. Patent 5,153,050).

Gerber et al. is described in full detail above. As noted above, Gerber et al. appear to teach bonding the plurality of single circuit board layers to upper and lower outermost copper conductor layers to form an integral multilayer circuit board (See in particular Figure 11). In the event this is not seen as an explicit teaching of an upper outermost conductor layer the following rejection is set forth. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the heating and pressing of an interconnect taught by Gerber et al. an upper outermost conductor layer (e.g. copper conductive pads on a circuit board) and layer of adhesive on the upper outermost insulating layer to form an integral, operable (i.e. electrically interconnected) multilayer circuit board substrate as was well known and conventional in the art as shown for example by Fukukawa et al. and/or it would have been obvious to one of ordinary

skill in the art at the time the invention was made to include in the heating and pressing of an interconnect taught by Gerber et al. an upper outermost conductor layer (e.g. copper conductive pads on a circuit board) and layer of adhesive on the upper outermost insulating layer to form a multilayer circuit board substrate that is protected from the environment as was well known and conventional in the art as shown for example by either one of Bohn or Johnston.

Fukukawa et al. disclose an integral multilayer printed wiring board comprising a circuit board substrate having conductive bumps (similar to that described by Gerber et al.) having upper and lower outermost copper foil conductive layers bonded to the circuit board substrate through a layer of adhesive (See the abstract).

Bohn and Johnston both disclose the well known and conventional method for forming a multilayer printed circuit board by providing a stack of printed boards layers, i.e. insulating layers having conductors thereon, placing outermost conductor layers on the stack, interposing adhesive layers between all of the individual layers, and laminating the stack to form multilayer printed circuit boards protected from the environment (Figure 1 and Column 1, lines 27-28 and Column 3, lines 49-58 of Bohn and Figure 1 and Column 1, lines 11-19 and Column 4, lines 23-57 of Johnston). Bohn additionally teaches that in forming a multilayer circuit board the internal circuit board structures may be any that are desired it being only essential that the outer sides are covered by conductor layers (Column 1, lines 27-28 and Column 3, lines 56-58).

Response to Arguments

5. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues Gerber et al. do not teach "stacking an outermost conductor layer made of a copper foil on an insulating layer side of a first outermost printed board with a bonding layer being interposed therebetween". This argument is addressed above in paragraph 3, see in particular Figure 11 of Gerber et al. Applicant further argues "an ordinarily-skilled artisan seeking to provide for the delivery of electrical signals through the multi-layer circuit board of Gerber to an outer layer would not have looked to the teachings of Bohn, which only shows the use of metal layers for environmental protection." It would have been obvious to one of ordinary skill in the art to provide an upper outermost copper layer in Figure 9 of Gerber et al. to provide environmental protection as suggested by Bohn. Furthermore, an additional rejection over Gerber et al. in view of Fukukawa et al. is made above to show the known technique of outer copper layers to provide for the delivery of electrical signals in a multilayer circuit board.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Blaine Copenheaver can be reached on (571) 272-1156. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John L. Goff

BLAINE COPENHEAVER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700